

PCB 75017 and PCB 75018

3.1 Introduction

All the controls of the MJS401D, with the exception of the POWER on/off switch and the MONITOR level control, have their outputs fed to the microcomputer. The microcomputer processes their signals, decides on the appropriate action, indicates to the front panel the settings of the instrument, and controls the signal electronics. It switches signal paths, gains and tuning of filters. It also measures the frequency and level of various signals in the system, and takes appropriate action. Finally, if a remote control interface is fitted, it receives commands, decodes them, acts on them, measures results, encodes them into a form suitable for the remote system, and transmits them.

3.1.1 CPU, EPROM, RAM

The microcomputer is a Z80A running at 4 MHz clock rate. One or two 8K x 8 EPROMs, type 2764, are addressed at 0000-1FFF and 2000-3FFF. One 2K x 8 RAM is addressed at 8000-87FF.

3.1.2 Parallel I/O

Sixteen ports at I/O locations 10 to 1F are addressed. All of them are D-type latches, type 74HC374. Four are on the front panel PCB and one is in the MD404B oscillator. The remaining eleven are on the microcomputer PCB.

Six input ports at I/O locations 10, 12 to 14, 16 and 17 are addressed. These are 74HC244 buffers. Those at locations 13 and 16 are four bits, the remainder are eight bits.

3.1.3 Clock and timebases

A quartz crystal runs at exactly 8 MHz, trimmed by VC1. This frequency is divided down to binary submultiples for various uses. 4 MHz is used to feed the Z80A CPU and the CPU of the MD404B oscillator. 500 kHz is used as the timebase for the frequency counter and as the clock for the A-D converter. More binary division stages produce an interrupt to the CPU every 16384 microseconds, which runs the time-sharing executive programme to schedule all the computer's programmed tasks.

3.1.4 Frequency counter

Five input signals can be fed, via a trigger conditioning circuit, to a frequency counter. This is of a special type which times an exact number of cycles and divides the number by the time to produce a result which tends to a proportionally constant accuracy.

3.1.5 Analogue to digital converter

Five input signals can be measured by a ten-bit A-D converter. This is of the successive approximation type, with internal reference voltage. Clocked at 500 kHz, it converts in a little over 20 microseconds.

3.1.6 Crosstalk input stage

A high-quality balanced input stage provides an input for external signals to the frequency counter.

3.1.7 Meter LED drivers

A one-of-four decoder with enable provides current for the LEDs in the analogue meter, to indicate which scale is in use. The enable is used to flash LEDs.

3.1.8 Remote-control interface

Full information on these is contained in Chapter 14 (IEEE/GPIB) or Chapter 15 (serial). The microcomputer provides lines to address devices at I/O locations 20 to 3F, and will accept interrupts from them. Power is provided at $\pm 18V$ and +5V. Access is via connector CONN3.

3.1.9 HALT LED

An LED, D7, is illuminated when the CPU is halted (task finished, awaiting the next interrupt). This is a useful indicator of the health of the microcomputer.

3.2 Circuit description

3.2.1 Clock generator and timebases

TR1, X1 and their associated components form an oscillator at 8 MHz, the fundamental of X1. The basically sinusoidal output is buffered and converted to 5V levels by TR2 and TR3. IC3, a 4-stage binary divider, produces outputs with 50 % duty cycle at 4 MHz, 2 MHz, 1 MHz and 500 kHz. The 4 MHz output feeds the CPU, IC10, and, via IC9 pins 3 and 4, provides a buffered output to the CPU of the MD404B oscillator.

The 500 kHz signal is further divided by IC4, a binary divider. At IC4 pin 2 is a square wave with a period of 16384 us. Every rising edge causes IC5 pin 8 to go low, causing an interrupt to the CPU.

3.2.2 Reset Circuit

IC1 pins 10/11/13 is a comparator. A simple reference voltage of around 1.5 V is developed by R4 and D2. C1 charges up slowly via R1. While the voltage on C1 is low, IC1 pin 13 is held low, sending an active-low reset signal to the CPU.

R3 and R5 apply a little positive feedback to ensure a clean exit from the reset state.

When the voltage on the +5V line falls, D1 rapidly discharges C1 to ensure a reset when the power is next restored.

3.2.3 CPU, EPROM, RAM

IC10 is an NMOS Z80A CPU. IC12 and IC13 are 8K x 8 EPROMS, type 2764. IC11 (74HC138) decodes addresses to chip-select the EPROMS in 8K blocks. The expression for chip select is:

Address.MREQ.RD.(NOT RFSH)

The active-low RD (read) signal is also fed to the EPROM active-low OE (output enable) pins.

IC12 is addressed from 0000 to 1FFF; IC13 is from 2000 to 3FFF.

IC14 is a 2K x 8 static RAM, type 6116 or its NMOS equivalent. IC15, IC9 and IC45 perform decoding to address it at 8000 to 87FF. The logical expression for chip select is:

Address.MREQ.(NOT RFSH)

The active-low RD signal is applied to the RAM OE pin, and the active-low WR signal is applied to the RAM WE (write enable) pin.

NMI (Non-Maskable Interrupt) and BUSRQ (Bus Request) are not used, and are pulled passive high by R37 and R38 respectively.

3.2.4 Interrupts

Interrupts (maskable) are received from IC47 pin 3. Since both inputs and the output are active-low, this gate functions as an OR gate, i.e. it signals interrupt to the CPU when either or both of its inputs is low. Interrupts are received from two sources; the timer and the remote control interface.

The timer generates an active-low interrupt every 16384 us at IC5 pin 8. This source is polled by a read of bit 5 of input 16, and cleared by performing a read of input port 15. No data is actually input from port 15; the input line merely resets IC5 at pin 13. This reset input is asynchronous and active-low.

The remote-control interface generates an active-low interrupt at IC47 pin 2. This source is polled by a read of bit 4 of input port 16. In the absence of a remote-control interface, R27 pulls this interrupt line passive high.

3.2.5 Wait

One source of wait states is the A-D converter, IC16. Its STATUS line, pin 14, is low when busy and high when not busy, i.e. conversion complete. IC47 pin 6 goes low during a read of either input port 16 or 17, which are the two ports to input data from the ADC. If a read of 16 or 17 is performed when STATUS is busy, IC45 pin 6 goes low, taking IC47 pin 8 low. This causes the WAIT line (IC10 pin 24) to go active low. The input strobe line will remain low until after the STATUS line has gone high to signal end of conversion, whereupon the WAIT line will go high again, and the read operation will be completed.

The other source of wait states is the oscillator communications port. When a byte is written to the oscillator (port 1F), the oscillator pulls connector 1 pin 116 low until after it has read the byte. If another write is performed to port 1F before connector 1 pin 116 has been returned high, IC45 pin 8 goes low, causing IC47 pin 8 to go low and pull the WAIT input of IC10 active low. When the oscillator has read the byte, IC45 pin 10 is set high, causing IC47 pin 8 to go high and remove the wait states.

3.2.6 I/O Bus

IC26 (74HC245) is a bidirectional bus buffer. On the B side are the CPU, EPROMS and RAM. On the A side are all the input and output ports.

In order to maintain adequate data hold time, the enable input of IC26 is held active for a short time after the end of the I/O request. This is controlled by IC48 (74HC74), a D-type flip-flop. The active-low IORQ signal from the CPU immediately sets IC48, whose output pin 8 goes low and enables IC26. When IORQ returns high, IC26 is not reset until the next positive transition of the CPU clock. This is approximately 1/2 clock cycle later.

The signal to the direction input of IC26 also has to be extended. This is performed by an S-R latch constructed (unusually) from one AND gate and one OR gate. The latch is not set on I/O read (input) cycles. On I/O write (output) cycles, the active-low WR signal from the CPU causes IC47 pin 13 and therefore IC47 pin 11 to go low. IC48 pin 8 has been set low by IORQ, therefore IC45 pin 3 goes low. This state will be maintained after WR has gone high again, and will be terminated by IC45 pin 8 going high.

3.2.7 Parallel I/O

IC27 performs the first level I/O decoding. Address lines A3 to A5 decode into blocks of 8 addresses. Address lines A6 and A7 must be low, and M1 from the CPU must not be active, to produce an output from IC27.

IC28 and IC41 complete the decoding for output ports 10 to 17 and 18 to 1F respectively. WR from the CPU must be active, along with one output of IC27, and IORQ (returned to active-high by IC9 pins 5 & 6). The complete logical expression for an output of IC28 or IC41 is:

Address.IORQ.WR.(NOT M1), inverted.

IC44 completes the decoding for input ports 10 to 17. Address lines A0 to A2 complete the address decoding. RD from the CPU must be active, along with one output of IC27, and IORQ from the CPU. The complete logical expression for an output of IC44 is:

Address.IORQ.RD.(NOT M1), inverted.

Address decoding from the 256 possible simple I/O ports is complete. Reads are performed by a simple level-sensitive enable of the appropriate 3-state buffer, type 74HC244. Writes are to D-type latches, and occur on the rising (trailing) edge of the output strobe line, giving the maximum possible data setup time.

3.2.8 A-D converter

IC16 (ZN432E) is a 10-bit successive approximation A-D converter with internal reference. Its clock, at 500 kHz, is derived from the quartz crystal X1 via divider IC3.

The timing requirements for the active-low Start Conversion pulse are satisfied by IC46, IC21 and IC48. The command to start conversion is initiated by performing a read of location 11. No data is input, but IC44 pin 14 pulses low. The two sections of IC46 are configured as an S-R latch. IC46 pin 3 goes high. Since IC48 pin 6 is normally high, IC46 pin 4 goes low, causing IC21 pin 11 to go low and issue a Start Conversion to the A-D converter.

On the next rising edge of the 500 kHz clock, IC48 pin 6 goes low. This maintains IC21 pin 11 low, and causes IC46 pin 4 to go high.

The output strobe pulse is nominally 625 ns wide, and returns high when ended. IC46 pin 3 goes low, and maintains IC46 pin 4 high.

One 500 kHz clock pulse later, IC48 pin 6 goes high again. The Start Conversion pulse has been between 2 us and 4 us wide, ending on a rising edge of the A-D converter clock.

As soon as the Start Conversion pulse is applied, the Status output at IC16 pin 14 goes low to indicate "busy". This pin returns to a high level 10.5 clock cycles (21 us) after the end of the Start Conversion pulse.

Parallel data are presented at the outputs B9 (MSB) to B0 (LSB). IC24 and IC25 serve as 3-state buffers to the I/O bus.

IC49 (4051B) selects one of five analogue inputs. These are normally in the range 0V to +10V. IC49 is therefore powered from 0V and +18V, and the three control inputs on pins 9, 10 and 11 have to be level-shifted. IC1 (LM339) is used for pins 10 and 11. TR10 (BC182LB) is used for pin 9. The three bits are derived from output port 17, bits 2, 3 and 4. C12 - C15 and C30 decouple HF noise on analogue inputs, which could cause false readings. IC8 pins 1, 2 & 3 is connected as a unity-gain buffer to feed the relatively low resistance of the analogue components of the ADC. VR3 adjusts the zero, and VR4 the full scale or span, of the ADC.

3.2.9 Frequency counter

IC6 (4051B) selects one of five signal inputs. Since these signals are A.C. and centred on 0V, IC6 is powered from ± 5 V. Bits 5, 6 and 7 of output port 1D select the input.

The selected input is fed into an AGC amplifier consisting of IC7 and IC8 pins 5, 6 & 7, with TR4 as the active gain-control element. The output signal from IC7 is inverted at unity gain by IC8. Diodes D5 and D6 provide a full-wave rectified signal, through the peak hold network R26, C10 and R24, to the gate of TR4 to cause it to attenuate the signal. The result is that the signal at IC7 pin 6 remains at about 2V to 3V peak to peak over a wide range of input levels.

This signal is converted to a square wave in IC1 pins 2, 4 and 5, which is a comparator with substantial positive feedback via R34. The effect of this is to cause hysteresis of approximately 25 %, which considerably improves the immunity to false triggering from noisy signals. Since the hysteresis is applied to a signal of a well regulated level, the hysteresis is almost constant.

The square wave at the incoming signal frequency, from IC1 pin 2, is gated and fed to the timer and counter circuits, IC22 and IC23.

The frequency counting process begins with a reset pulse from bit 2 of output port 14, which resets IC17, IC18, IC20 and IC22. The D input pin 5, of IC17, is at logic 1. IC9 pins 1 and 2 inverts the signal to be measured. The first positive transition at IC9 pin 2 after the reset signal has ended, clocks a logic 1 through to IC17 pin 1. This is a negative transition of the incoming signal. The next positive transition clocks the logic 1 through to IC17 pin 13. This is the gate signal; the gate is now open. Positive transitions of the incoming signal, gated by IC21 pins 4, 5 and 6, are counted in IC20 (4534B), a 5 decade counter. Similarly, positive transitions of 500 kHz clock, gated by IC21 pins 1, 2 and 3, are counted in IC22 (4534B).

After 100 000 counts in IC22, which is exactly 200 ms, IC22 pin 13 goes high for one cycle of 500 kHz. A logic 1 is clocked into IC18 pin 1, and a 0 into IC18 pin 2. On the next negative transition of the incoming signal, this logic 0 is clocked into IC17 pin 1. On the next positive transition, the logic 0 is clocked into IC17 pin 13. The gate is now closed.

If the incoming signal is at 500 kHz or more, IC20 pin 13 will cause a logic 1 to be clocked into IC18 pin 13. This signals to the microcomputer that the frequency is too high.

The result of the counting process is a number of cycles in IC20, and the number of cycles of 500 kHz clock, less 100 000, in IC22 which occurred from positive transition to positive transition of the counted cycles of the input signal.

The 4534B was designed for direct display drive. Its outputs, therefore, are multiplexed, and it contains a "scanner" which activates one line for each of the five decade stages which it scans. Both the BCD and scanner outputs are three-state, with active-low enable inputs. IC19 (4556B) selects the four possible outputs:

- (1) BCD data from IC22.
- (2) Decade select from IC22.
- (3) BCD data from IC20.
- (4) Decade select from IC20.

Bits 0 and 1 of output 14 select one of the above. Bit 2 resets the counters, overflow flags and gate. Bit 3 clocks the scanner to get data from the next decade. Bit 4 resets the scanner to a known state.

Input port 14 reads the data and status from the frequency counter system. Bits 0 to 4 are BCD data or a decade select strobe, bit 5 is the time carry output, bit 6 is the overflow from the number of cycles counter, and bit 7 is the gate.

3.2.10 Balanced input stage

IC2 (NE5532) forms a high quality balanced input stage. Input impedance is defined by R15 and R16 at 100 K, the inverting inputs of IC2 both being at virtual earth. Common mode rejection is adjusted at low to medium frequencies by VR1, and at high frequencies by VR2.

IC2 pins 5, 6 and 7 invert the incoming live or in-phase signal and reduce its level, to maintain an adequate common mode range. IC2 pins 1, 2 & 3 add this to the incoming return or anti-phase signal, thus producing a differential amplifier. R21 sets the stage gain at unity. D3 and D4 clip the signal at about ± 9 V so that the return signal cannot overload IC2 and thereby feed through to the live input. D3 and D4 are actually base-emitter junctions of transistors, which have a much lower capacitance than ordinary zener diodes, and therefore do not reduce the H.F. response of the IC2 stage excessively.

The output of this stage is fed via C9 to the frequency counter input multiplexer.

3.2.11 Halt LED

TR5 drives D7, a red LED, when the processor is halted. The processor halts when it executes a HALT instruction. This is reached when the tasks have all been completed and nothing remains to be done before the next interrupt. Only an interrupt can free the CPU from the halted state.

3.2.12 Meter LED drivers

IC19 pins 9-12 drive emitter followers TR6 - TR9, which drive the four LEDs in the meter movement. Bits 6 and 7 of output 17 cause IC19 to select one LED. Bit 5, if high, deselects all LEDs. This is used to cause an LED to flash.

3.2.13 Power Supplies

All the digital ICs are powered from the +5V line, which is decoupled by C20, C22, C23, C25, C28, C29 and C33. The $\pm 18V$ lines are decoupled by R40/C31 and R42/C32 for IC2, R41/C26 for IC1, IC7 and IC8, and R43/C27 for IC7 and IC8. A -5 V line is derived by IC33 (7905) for IC6 and IC16.

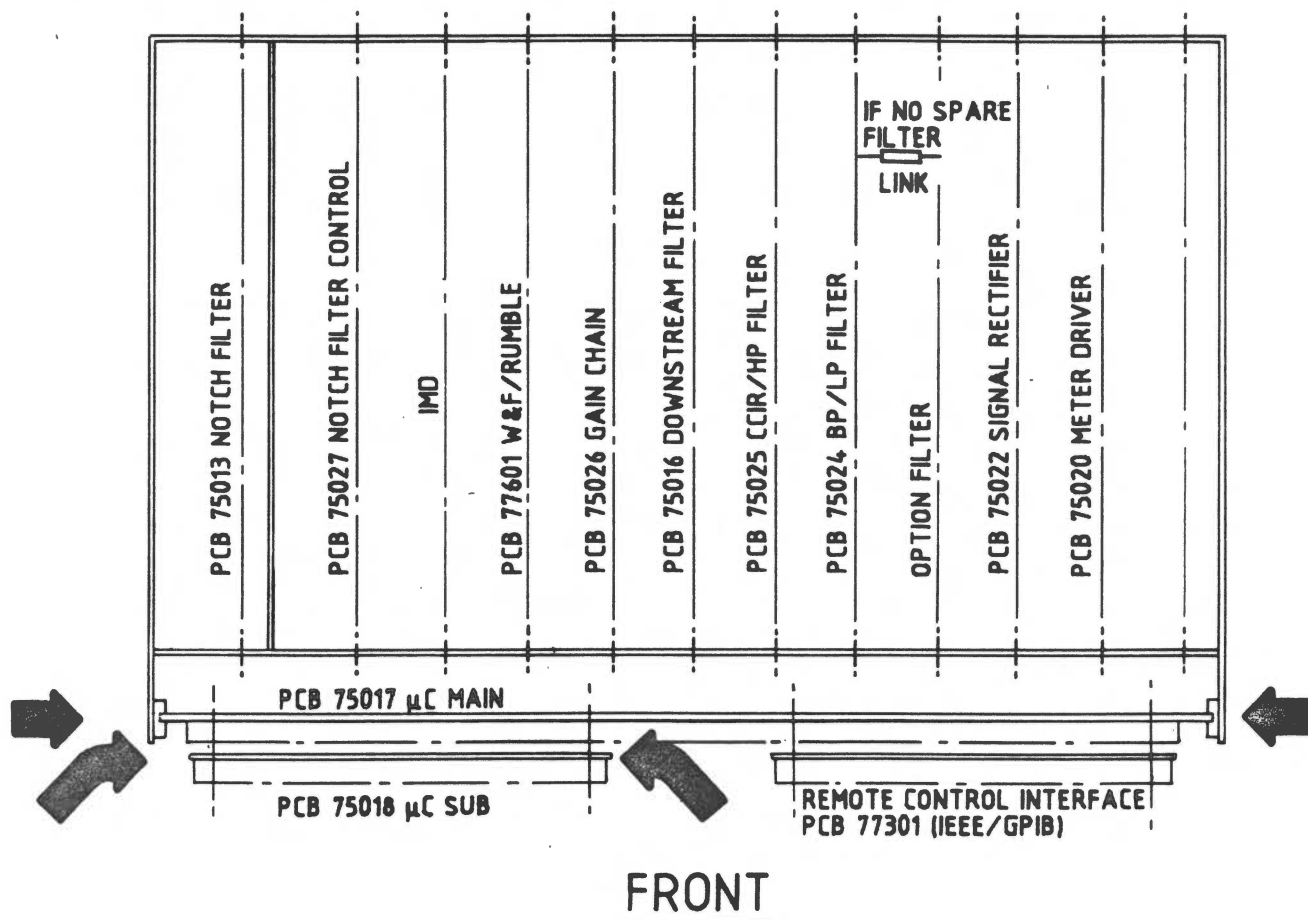
3.3 Removal/Replacement

3.3.1 Removal

Turn off the MJS401D and remove the mains lead.

Remove the four screws retaining instrument top cover. Pull the top cover straight up.

The microcomputer system assembly is located across the front of the main card frame inside the instrument - directly behind the front panel.



MJS401D PCB Location Guide

First, unplug the ribbon cable connecting this to the front panel PCB. Fold cable forward over the front of the case.

To remove, pull up on the corners. It will probably be necessary to ease it slowly one side at a time due to the large number of contacts.

If an optional Bus Interface Card is fitted (piggy-back PCB on right hand side) then there will be one or two ribbon cables running from the right side of this board to the rear of the case. Unplug these if necessary to extract the Microcomputer PCB.

3.3.2 Sub-board

The sub-board is hard wired to the main PCB and can be accessed by removing the four retaining screws and swinging upward.

In some cases the wiring between the two PCBs consists of individual wires. Exercise care not to flex these repeatedly to avoid failure.

3.3.3 Remote Control Interface Card

Full information on these is contained in Chapter 14 (IEEE/GPIB) or Chapter 15 (serial).

The Interface card connects to the rear panel by a ribbon cable running between the oscillator housing and Main Card Frame. This cable plugs into the right side of the Remote Control Interface Card.

The Interface Card connects to the Microcomputer via CONN 3, the LOWER of the 26 way headers.

To remove the Interface Card, unplug both connectors, and remove the 4 fixing screws.

3.3.4 Extender Assembly

To ease fault finding, an Extender Assembly is available. To use it, install with the socket contacts downward and test points facing forward.

Push it down carefully into the guides. Visually confirm that the sockets on the bottom of the extender align with the pins on the Motherboard, especially at the centre of the card. Failure to do this may result in bent or broken contacts. When fully down the card will snap into position.

3.3.5 Reassembly

Replace 4 screws retaining Sub-board to main Microcomputer PCB. Use low-strength thread locking compound, e.g. Bostik T22.

Fit Interface Card (if required) by replacing the 4 fixing screws. Use low-strength thread locking compound. Plug 26 way ribbon on interface card into CONN 3, the LOWER header on the main Microcomputer PCB. The other ribbon cable from the socket on the rear of the chassis plugs into the side of the Interface Card.

Slide the Microcomputer PCB down carefully in its guides. Before pressing completely down check to see that the connectors in the centre of the PCB are properly aligned with the pins on the Motherboard. Failure to do this may result in bending or breaking the connector pins.

Also ensure that front panel wiring does not interfere with the PCB.

Push the PCB fully down - it should snap into place.

Plug the 26 way ribbon cable connector from the front panel into CONN 2, the UPPER header on the main microcomputer PCB.

3.4 Fault Finding

It is an interesting contradiction of modern semiconductor device production that the most complex devices are the ones least likely to fail. Therefore it is wise not to suspect the CPU, EPROM and RAM until all other possibilities have been exhausted.

3.4.1 Partial malfunctions

A partial malfunction of the microcomputer, e.g. one line stuck but everything else working, is best cured by reference to the circuit description. Look for logic levels coming out of all CMOS ICs accurately at 0 V or +5 V. Intermediate states indicate a fault, which could be either in the device generating the state, or in the input stage(s) of the device(s) receiving the signal.

Always use a low-capacitance probe (x10 or similar), grounded to a point near the source of the signal to be measured. The capacitance of a x1 probe or a simple coaxial cable may upset the operation of the system by substantially increasing rise and fall times. Simply grounding the probe to the chassis of the MJS401D will cause all manner of digital and R.F. noise to be picked up, and may mislead one into thinking that there is a problem, which in reality does not exist.

3.4.2 Major malfunctions

If everything stops working.

Check that all four supply rails are present and correct.

Check for the presence of a good 4 MHz waveform at IC10 pin 6.

If not: Check the crystal oscillator stage, TR1 to TR3.

Check the divider, IC3.

Check for 500 kHz at IC16 pin 7.

If not: As above.

Check that the reset line, IC10 pin 26, is briefly low on switch-on but goes to +5 V immediately afterwards and stays there.

If not: Check the reset circuit, IC1 pins 10, 11 and 13.

Check that the wait line (IC10 pin 24) is high.

If not: Check for 500 kHz at IC16 pin 17.

Check that the Start Conversion line (IC16 pin 28) is high.

This should only pulse low briefly. If it stays low, the Status line will stay low and cause an infinite wait state.

Check that the Status line (IC16 pin 14) is high.

Check around IC47 pins 4, 5, 6, 8, 9, 10; IC45 pins 4, 5, 6, 8, 9, 10.

Check that the INT line (IC 10 pin 16) is mostly high, pulsing low every 16 ms approx. The duration of the low pulse will vary a lot but should never be more than a few hundred microseconds.

3.5 Calibration

The Microcomputer system needs little calibration. It is only necessary to set up the clock frequency (which is critical for the frequency measurement system), the common mode rejection of the audio input to the frequency measurement system, and the A/D converter.

This calibration procedure requires:

(i) a frequency counter of at least 6 digits resolution and with a timebase error of 10 parts per million or better;

(ii) a digital voltmeter of at least 4 1/2 digits resolution and an accuracy of 0.05 % or better. An ordinary 3 1/2 digit DVM is almost certainly NOT sufficiently accurate;

(iii) a signal generator with sine wave output of up to +10 dBu at 1 kHz and 10 kHz. Note that the MD404B, if fitted, CANNOT be used for this test because the output must be fed into the microcomputer in common mode, but is permanently wired in differential mode within the instrument. If you have another MJS401D with MD404B, it may be used as the source;

(iv) an oscilloscope.

If the frequency counter and/or DVM were calibrated more than 6 months ago, have them calibrated by a laboratory with traceable standards before using them to calibrate the MJS401D.

3.5.1 Clock Frequency

Using the frequency counter, measure the frequency at LK1 (near Z80 CPU).

Adjust VC1 (on the sub board, PCB75018) until the frequency is exactly 4.000 000 MHz. If the extender PCB is not used, it will be necessary to remove the front panel to access the adjuster of VC1.

If the front panel was removed, replace it.

3.5.2 A/D Converter

Switch MJS401D off.

Depress "LEVEL" and hold while switching MJS401D back on for DIAGNOSTICS.

Depress "LEVEL" again. Display will show GROUP 1. Depress "X-TALK".

Apply 10 mV D.C. to Pin 22 on the extender.

Adjust VR3 until display reads "ADC 004".

Apply 10 V D.C. as above.

Adjust VR4 until display reads "ADC FA0".

Press OPTION A to return to DIAGNOSTIC, then LEVEL followed by CCIR 468 to return to normal operation. (NB Earlier issues of software do not have this reset facility, so for these versions it will be necessary to turn the POWER switch off and on again.)

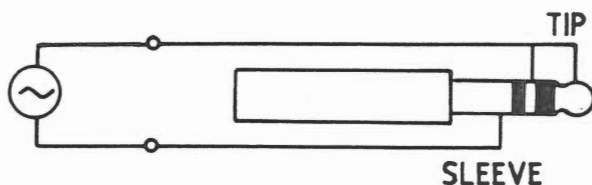
3.5.3 Frequency Measurement System - CMRR Adjustment

If an MD404B oscillator is fitted, select "MUTE" and "600".

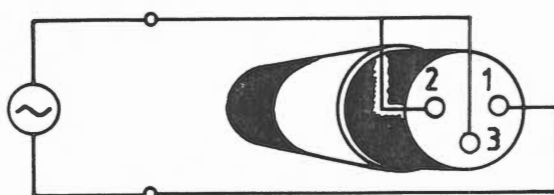
The source will be FED INTO the "OSCILLATOR" output sockets on the right of the instrument.

Connect the "IN-PHASE" and "ANTI-PHASE" poles of the MJS401D "OSCILLATOR" connector together and drive between these and ground as shown below.

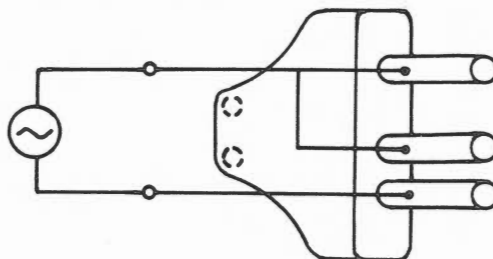
In the JACK Version:



In the XLR Version:



In the EURO Version:



Short out R10 to reduce noise (disables clock generator).

Connect the oscilloscope to TP1.

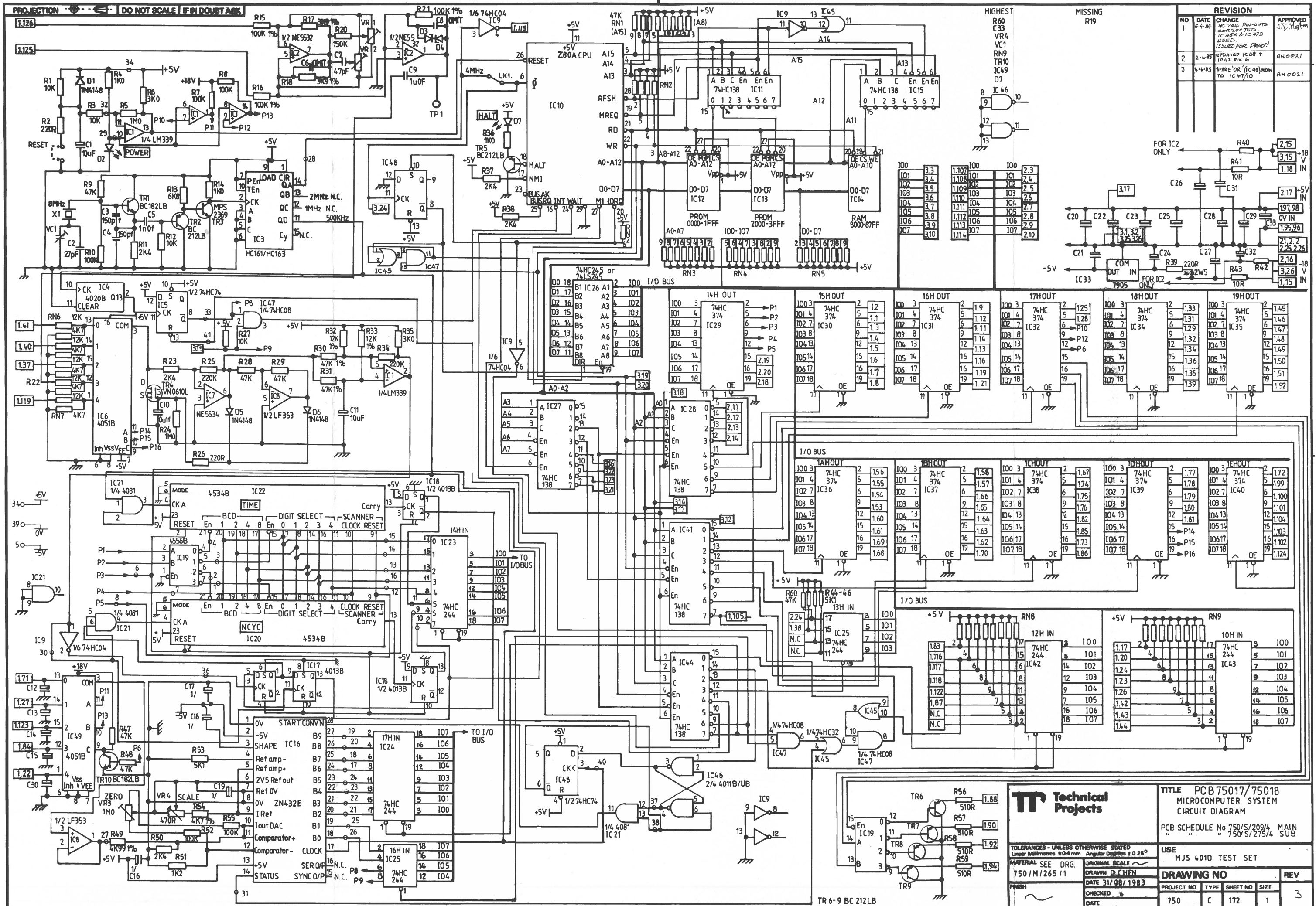
SINE SOURCE

STEP	FREQ	LEVEL		ADJUST	FOR
		dBu	VOLTS		
1	1 kHz	~+10	~2.5	VR1	Minimum 1 kHz trace
2	10 kHz	~+10	~2.5	VR2	Minimum 10 kHz trace
3	Repeat 1 and 2 until best result is obtained.				

Remove the short from R10. Power the MJS401D down and up again to reset the microcomputer.

3.5.4 Check Frequency Counter System

Use an ordinary lead (not the special common-mode rejection test lead above) to input a signal from the sine source to the MJS401D and the frequency counter. Set sine source to 1.000 kHz using the frequency counter. Confirm that the frequency readout on the MJS401D is between 999 Hz and 1.001 kHz.



REVISION				
NO	DATE	CHANGE	APPROVED	
1	5-4-84	HC 244 PIN-OUTS CORRECTED. IC 454 & IC 470 USED. ISSUED FOR PRODUCTION	SS. High	
2	2-4-85	UPDATED IC 454 & IC 470 TO 10-4-70	AN0021	
3	4-4-85	SPARE OR (IC 454) NOW TO 10-4-70	AN0021	

Technical Projects

TOLERANCES - UNLESS OTHERWISE STATED
Linear Millimetres ±0.4mm Angular Degrees ±0.25°

MATERIAL SEE DRG. 7501M/265/1

DATE 31/08/1983

CHECKED

DATE

TITLE PCB 75017/75018
MICROCOMPUTER SYSTEM
CIRCUIT DIAGRAM

PCB SCHEDULE No 750/S/209/4 MAIN
" " 750/S/275/4 SUB

USE MJS 4010 TEST SET

DRAWING NO	PROJECT NO	TYPE	SHEET NO	SIZE	REV
750	C	172	1		3